|  |  |  |  |
| --- | --- | --- | --- |
| operation | regWrite | selOp | destSrc |
| load | 1 | 000 | 00 |
| mov | 1 | 000 | 01 |
| add | 1 | 000 | 10 |
| sub | 1 | 001 | 10 |
| and | 1 | 010 | 10 |
| or | 1 | 011 | 10 |
| xor | 1 | 100 | 10 |
| store | 0 | 000 | 11 |

Control Signals:

ALU operations:

|  |  |
| --- | --- |
| operation | selOp |
| add | 000 |
| sub | 001 |
| and | 010 |
| or | 011 |
| xor | 100 |

Mux select:

|  |  |
| --- | --- |
| operation | sel |
| dataIn | 00 |
| dataA | 01 |
| ALUout | 10 |
| dataB | 11 |